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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,201	MOON, SEUNG-HWAN	
	Examiner	Art Unit	
	Jason M. Mandeville	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 10-15* is/are rejected.

7)☒ Claim(s) *3 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10 October 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 4 and 8-9** are cancelled.

Claim Objections

2. **Claim 3** is objected to because of the following informalities: the claim is amended, but is labeled as "Original". Appropriate correction is required.

3. **Claim 12** is objected to because of the following informalities: amendments made in the claim are not underlined. In the last line of the claim, the word "or" has been replaced with the word "and", yet the word "and" has not been underlined to show this amendment. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 1-3, 5-7, and 10-15** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter

which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. **Claim 1** recites a liquid crystal display comprising a timing controller that "does not provide the nth image data to the data driver when all bits of the nth image data and the (n-1)th image data are equal and complimentary." Similarly, **Claim 12** recites a driving method of a liquid crystal display wherein the method comprises "providing data voltages corresponding to the nth image data to the data line when at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal and complementary to each other." As pertaining to **Claim 1**, it is unclear from the specification and the associated drawings how "all bits of the nth image data and the (n-1)th image data" can be both "equal and complementary to each other." The term "equal" implies that all of the bits of the (n-1)th image data are the same as all of the bits of the nth image data, whereas the term "complementary" implies that all of the bits of the (n-1)th image data are the opposite of all of the bits of the nth image data (i.e., a "0" in the nth image data corresponds to a "1" in the (n-1)th image data, and a "1" in the nth image data corresponds to a "0" in the (n-1)th image data). Thus, it is impossible for all of the bits of the nth image data and the (n-1)th image data to be equal. Similarly for **Claim 12**, it is unclear what is meant by the limitation that data voltages are provided corresponding to the nth image data when "at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal and complementary to each other." Again, the term "equal" implies that all of the bits of the (n-1)th image data are the same as all of the bits of the nth image data,

whereas the term "complementary" implies that all of the bits of the (n-1)th image data are the opposite of all of the bits of the nth image data (i.e., a "0" in the nth image data corresponds to a "1" in the (n-1)th image data, and a "1" in the nth image data corresponds to a "0" in the (n-1)th image data). Thus, it is unclear what condition must be met to provide the nth image data to the data line. As such, it is unclear what level of experimentation is necessary to implement the liquid crystal display and driving method as disclosed by **Claims 1 and 12**.

Claims 2-3, 5-7, 10-11, and 13-15 are rejected as being dependent from **Claims 1 and 12**.

6. **Claims 1-3, 5-7, and 10-15** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. **Claim 1** recites a liquid crystal display comprising a timing controller that "does not provide the nth image data to the data driver when all bits of the nth image data and the (n-1)th image data are equal and complimentary." Similarly, **Claim 12** recites a driving method of a liquid crystal display wherein the method comprises "providing data voltages corresponding to the nth image data to the data line when at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal and complementary to each

other." As pertaining to **Claim 1**, the limitation that "all bits of the nth image data and the (n-1)th image data" are both "equal and complementary to each other" is not disclosed in the original specification. Similarly for **Claim 12**, the limitation that data voltages are provided corresponding to the nth image data when "at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal and complementary to each other" is not disclosed in the original specification. As such, **Claims 1 and 12** contain new matter.

Claims 2-3, 5-7, 10-11, and 13-15 are rejected as being dependent from **Claims 1 and 12**.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1-3, 5-7, and 12-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki et al. (hereinafter "Hiraki" US 6,680,722) in view of Mizumaki (US 6,333,727).

9. As pertaining to **Claim 1**, Hiraki discloses a liquid crystal display (see Fig. 3, Fig. 4, and Fig. 5) comprising: a liquid crystal panel assembly (40) including a plurality of gate lines (12), a plurality of data lines (13) which are insulated from and intersects the gate lines (12; see Col. 7, Ln. 48-53), and a plurality of pixels (herein referred to as picture elements) each of which is formed in an area defined by a data line (13) of the data lines (13) and a gate line (12) of the gate lines (12) and has a switching element (15) connected to the gate line (12) and the data line (13; Col. 7, Ln. 41-67);

a gate driver (34) for supplying gate voltages (Scan, Col. 9, Ln. 55-58) to the gate lines (12);

at least one data driver (33) for supplying data voltages (Col. 9, Ln. 46-54) corresponding to image data (RGB) to the data lines (13); and

a timing controller (31).

Hiraki does not explicitly disclose that the timing controller (31) is utilized for comparing nth image data applied from outside and (n-1)th image data stored therein and selectively providing the nth image data to the data driver (33) depending on the comparison result, wherein the timing controller does not provide the nth image data to the data driver when all bits of the nth image data and the (n-1)th image data are equal or complementary to each other (the examiner assumes that the limitation is "equal or complementary", as opposed to "equal and complementary", which is not enabled).

However, Mizumaki discloses an image display method (see Fig. 1 and Fig. 3) in which a liquid crystal display device is driven by a memory controller (5) in order to reduce power consumption and to reduce screen flicker. In this configuration, input image data (C) from a current frame, stored in a first memory (3), is compared with image data from the previous frame, stored in a second memory (4) in order to determine whether the current image data (C) to be displayed differs from the previous image data. When the current image data (C) differs from the previous image data stored in the second memory (4), the second memory is rewritten with the current image data (C) and provided to the display. However, when the current image data (C) does not differ from the previous image data stored in the second memory (4), the image data stored in the second memory (4) is not rewritten with the current image data and the previous image data stored in the second memory (4) is again provided to the display. The memory controller (5) as shown in Fig. 3 serves as a comparator for the current image data and the previous image data and as a timing controller for reading and writing the current and previous image data into memory. Because it is a collective goal of Mizumaki and Hiraki to reduce power consumption, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the display panel driving method and data driver (33) taught by Hiraki with the first and second memory structure (3,4) taught by Mizumaki, as well as the timing controller (31) taught by Hiraki with the memory/timing controller (5) taught by Mizumaki, in order to produce a timing controller (combination of Hiraki (31) and Mizumaki (5)) and data driver (combination of Hiraki (33) and Mizumaki (3,4)) utilized for comparing nth image

data (i.e., current image data) applied from outside (i.e., applied from an outside image source such as a PC; see (37) in Hiraki and Mizumaki Col. 1, Ln. 21-25)) and (n-1)th image data stored therein (i.e., previous image data stored in the second memory (4) in Mizumaki) and selectively providing the nth image data to the data driver (33) depending on the comparison result (see Mizumaki Col. 5, Ln. 11-61, Col. 6, Ln. 55-67, Col. 7, Ln. 1-23, and Col. 8, Ln. 24-38).

Further, it would have been obvious to one of ordinary skill in the art that the combined teachings of Hiraki and Mizumaki disclose that (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) the timing controller (Hiraki (31) and Mizumaki (5)) does not provide the nth image data to the data driver when all bits of the nth image data and the (n-1)th image data are equal (i.e., the same) or complementary to each other (see Mizumaki Col. 5, Ln. 11-61, Col. 6, Ln. 55-67, Col. 7, Ln. 1-23, and Col. 8, Ln. 24-38; see Hiraki, Col. 9, Ln. 40-54, Col. 10, Ln. 61-67, Col. 13, Ln. 66-67 through Col. 14, Ln. 1-27).

10. As pertaining to **Claim 2**, Hiraki in view of Mizumaki discloses the liquid crystal display of claim 1 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3; see above rejection of claim 1) wherein the timing controller (Hiraki (31) and Mizumaki (5)) generates an operation control signal (i.e., an output of the timing controller to include read/write signals and polarity control) based on the comparison result (i.e., the comparison between the first memory (3) and the second memory (4)) and provides the operation control signal to the data driver (the data driver consists of the first and

second memory structures (3,4) of Mizumaki and the data driver (33) of Hiraki) and the data driver is operated with a mode, based on the operation control signal, selected from a holding mode (i.e., data is not written from first memory to second memory) which provides data voltages corresponding to the stored (n-1)th image data, an inverting mode (i.e., polarity of stored data is reversed) which provides data voltages corresponding to the inverted (n-1)th image data (in the instance that the first and second memories contain identical data, and the polarity controlling function (32; in Hiraki) inverts the polarity of the image data, the data driver will operate in the inverting mode), and an updating mode (rewrite second memory with first memory) which provides data voltages corresponding to the nth image data provided from the timing controller (see Mizumaki Col. 5, Ln. 11-61, Col. 6, Ln. 55-67, Col. 7, Ln. 1-23, and Col. 8, Ln. 24-38; see Hiraki, Col. 9, Ln. 40-54, Col. 10, Ln. 61-67, Col. 13, Ln. 66-67 through Col. 14, Ln. 1-27).

11. As pertaining to **Claim 3**, Hiraki in view of Mizumaki discloses the liquid crystal display of claim 2 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the timing controller (Hiraki (31) and Mizumaki (5)) includes:

a first line memory (3) for storing the nth image data applied from outside (i.e., current image data);

a second line memory (4) in which the (n-1)th image data applied in advance are stored (i.e., previous image data); and

a control signal generator (inherent within the timing controller) for generating an operation control signal (the operation control signal generated in the timing controller includes read/write control for the first and second memory units (3,4) and the polarity control (SCLK) that controls the polarity inversion) after comparing the nth image data (current image data) and the (n-1)th image data (previous image data); and

the control signal generator that generates (see Mizumaki Col. 5, Ln. 11-61, Col. 6, Ln. 55-67, Col. 7, Ln. 1-23, and Col. 8, Ln. 24-38; see Hiraki, Col. 9, Ln. 40-54, Col. 10, Ln. 61-67, Col. 13, Ln. 66-67 through Col. 14, Ln. 1-27):

an operation control signal of a first status to let the data driver operate with the holding mode (i.e., do not rewrite first memory (3) into second memory (4)) when all bits of the nth image data and the (n-1)th image data are equal to each other (Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38);

an operation control signal of a second status to let the data driver operate with the inverting mode (i.e., invert polarity) when all bits of the nth image data and the (n-1)th image data are complementary to each other (in the instance that nth image data and the (n-1)th image data are identical, and the polarity controller is activated by the control signal SCLK, the operation control signal will include holding the (n-1)th data (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38) and inverting the polarity of the (n-1)th image data (see Hiraki, Col. Col. 9, Ln. 40-54, Col. 10, Ln. 61-67, Col. 13, Ln. 66-67 through Col. 14, Ln. 1-27); in this way, the nth and (n-1)th data are complimentary to each other and the data driver will operate with the inverting mode); and

an operation control signal of a third status to let the data driver operate with the updating mode (i.e., rewrite the first memory (3) into the second memory (4)) when at least one bit (i.e., at least one significant bit) of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal or complementary to each other (Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38).

12. As pertaining to **Claim 5**, Hiraki in view of Mizumaki discloses the liquid crystal display of claim 3 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the timing controller (Hiraki (31) and Mizumaki (5)) generates an operation control signal whose status changes by 1H (one line period) period by comparing the nth image data and the (n-1)th image data during 1H period and the data driver holds, inverts, or updates the image data by 1H period (see above rejections; although neither Hiraki nor Mizumaki explicitly state that the operation control signal status is changed every 1H period, Mizumaki states that the control signal switches after "a time period during with such pixel data is input/output" (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38); it would have been obvious to one of ordinary skill in the art at the time when the invention was made that this time period implies a line period or 1H).

13. As pertaining to **Claim 6**, Hiraki in view of Mizumaki discloses the liquid crystal display of claim 3 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the timing controller (Hiraki (31) and Mizumaki (5)) generates an operation control signal whose status changes as many times as the number of the data drivers

by 1H period by comparing the nth image data and the (n-1)th image data for each data driver during 1H period and the data driver holds, inverts, or updates the image data for each data driver (see above rejections of claim 5 and claim 3; also, Hiraki teaches (see Fig. 5, Col. 8, Ln. 47-54) that the data driver (33) contains "a plurality of data driver IC", which implies a plurality of data drivers; it would have been obvious to one of ordinary skill in the art at the time when the invention was made that in order to drive the plurality of data driver ICs, the control signal status must change as many times as the number of data drivers).

14. As pertaining to **Claim 7**, Hiraki in view of Mizumaki discloses the liquid crystal display of claim 3 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the timing controller (Hiraki (31) and Mizumaki (5)) generates an operation control signal whose status changes as many times as the number of pixels of the line by 1H period by comparing the nth image data and the (n-1)th image data for each pixel during 1H period and the data driver holds, inverts, or updates the image data for each pixel (again, see above rejections; Mizumaki states that the control signal switches after "a time period during with such pixel data is input/output" (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38); it would have been obvious to one of ordinary skill in the art at the time when the invention was made that this time period implies a control signal change as many times as the number of pixels of the line).

15. As pertaining to **Claim 12**, Hiraki discloses a driving method of a liquid crystal display (see Fig. 3, Fig. 4, and Fig. 5), which includes a plurality of gate lines (12), a plurality of data lines (13) which are insulated from and intersects the gate lines (12; see Col. 7, Ln. 48-53), and a plurality of pixels (herein referred to as picture elements) each of which is formed in an area defined by a data line (13) of the data lines (13) and a gate line (12) of the gate lines (12) and has a switching element (15) connected to the gate line (12) and the data line (13; Col. 7, Ln. 41-67)), the method comprising:

providing data voltages according to image data to the data line (a data driver (33) supplies data voltages (Col. 9, Ln. 46-54) corresponding to image data (RGB) to the data lines (13)); and

making the data voltage be applied to the pixel by providing a gate voltage to the gate line (a gate driver (34) supplies gate voltages (Scan, Col. 9, Ln. 55-58) to the gate lines (12)).

Hiraki does not disclose that the provision includes comparing (n-1)th image data provided in advance and nth image data being provided currently; providing data voltages corresponding to the (n-1)th image data to the data line when all bits of the nth image data and the (n-1)th image data are equal to each other; inverting the (n-1)th image data and providing data voltages corresponding thereto when all bits of the nth image data and the (n-1)th image data are complementary to each other; or providing data voltages corresponding to the nth image data to the data line when at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are

not equal or complementary to each other (the examiner assumes that the limitation is "equal or complementary", as opposed to "equal and complementary", which is not enabled).

However, Mizumaki discloses these provisions in an image display method (see Fig. 1 and Fig. 3) in which a liquid crystal display device is driven by a memory controller (5) in order to reduce power consumption and to reduce screen flicker. In this configuration, input image data (C) from a current frame, stored in a first memory (3), is compared with image data from the previous frame, stored in a second memory (4) in order to determine whether the current image data (C) to be displayed differs from the previous image data. When the current image data (C) differs from the previous image data stored in the second memory (4), the second memory is rewritten with the current image data (C) and provided to the display. However, when the current image data (C) does not differ from the previous image data stored in the second memory (4), the image data stored in the second memory (4) is not rewritten with the current image data and the previous image data stored in the second memory (4) is again provided to the display. The memory controller (5) as shown in Fig. 3 serves as a comparator for the current image data and the previous image data and as a timing controller for reading and writing the current and previous image data into memory. Because it is a collective goal of Mizumaki and Hiraki to reduce power consumption, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the display panel driving method and data driver (33) taught by Hiraki with the first and

second memory structure (3,4) taught by Mizumaki, as well as the timing controller (31) taught by Hiraki with the memory/timing controller (5) taught by Mizumaki, in order to provide a timing controller (combination of Hiraki (31) and Mizumaki (5)) and data driver (combination of Hiraki (33) and Mizumaki (3,4)) utilized for comparing (n-1)th image data (i.e., previous image data stored in the second memory (4)) provided in advance and nth image data (i.e., current image data) being provided currently (see Mizumaki Col. 5, Ln. 11-61, Col. 6, Ln. 55-67, Col. 7, Ln. 1-23, and Col. 8, Ln. 24-38).

Further, Hiraki in view of Mizumaki discloses that the provision includes providing data voltages corresponding to the (n-1)th image data to the data line when all bits of the nth image data and the (n-1)th image data are equal to each other (i.e., do not rewrite first memory (3) into second memory (4)) when all bits of the nth image data and the (n-1)th image data are equal to each other (Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38); inverting the (n-1)th image data and providing data voltages corresponding thereto when all bits of the nth image data and the (n-1)th image data are complementary to each other (in the instance that nth image data and the (n-1)th image data are identical, and the polarity controller is activated by the control signal SCLK, the operation will include holding the (n-1)th data (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38) and inverting the polarity of the (n-1)th image data (see Hiraki, Col. 9, Ln. 40-54, Col. 10, Ln. 61-67, Col. 13, Ln. 66-67 through Col. 14, Ln. 1-27); in this way, the nth and (n-1)th data are complimentary to each other and the data driver will operate by inverting the (n-1)th image data); and providing data voltages corresponding

to the nth image data to the data line when at least one bit of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal or complementary to each other (i.e., at least one significant bit) of the nth image data and at least one corresponding bit of the (n-1)th image data are not equal or complementary to each other (Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38).

16. As pertaining to **Claim 13**, Hiraki in view of Mizumaki discloses the method of claim 12 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the provision compares the nth image data and the (n-1)th image data during 1H period (see above rejections; although neither Hiraki nor Mizumaki explicitly state that the operation control signal status is changed every 1H period, Mizumaki states that the control signal switches after "a time period during with such pixel data is input/output" (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38); it would have been obvious to one of ordinary skill in the art at the time when the invention was made that this time period implies a line period or 1H).

17. As pertaining to **Claim 14**, Hiraki in view of Mizumaki discloses method of claim 12 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the provision compares the nth image data and the (n-1)th image data for each data driver of the liquid crystal display during 1H period (see above rejections; also, Hiraki teaches (see Fig. 5, Col. 8, Ln. 47-54) that the data driver (33) contains "a plurality of data driver IC", which implies a plurality of data drivers; it would have been obvious to one of

ordinary skill in the art at the time when the invention was made that in order to drive the plurality of data driver ICs, the nth image data is compared to the (n-1)th image data for each data driver of the liquid crystal display during 1H period).

18. As pertaining to **Claim 15**, Hiraki in view of Mizumaki discloses the method of claim 12 (see Hiraki Fig. 3, Fig. 4, and Fig. 5; see Mizumaki Fig. 1 and Fig. 3) wherein the provision compares the nth image data and the (n-1)th image data for each pixel during 1H period (see above rejections; Mizumaki states that the control signal switches after "a time period during with such pixel data is input/output" (see Mizumaki, Col. 7, Ln. 46-67 through Col. 8, Ln. 1-38); it would have been obvious to one of ordinary skill in the art at the time when the invention was made that this time period implies a comparison of the nth and (n-1)th image data for each pixel during 1H period).

19. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki et al. (hereinafter "Hiraki" US 6,680,722) in view of Mizumaki (US 6,333,727) and further in view of Terukina et al. (hereinafter "Terukina" US 6,624,868).

20. As pertaining to **Claim 10**, Hiraki in view of Mizumaki disclose the liquid crystal display of claim 1. Hiraki teaches that the liquid crystal display has a structure such that a liquid crystal is sealed between two glass substrates (Col. 1, Ln. 29-48). However, Hiraki in view of Mizumaki does not explicitly state that the liquid crystal display has a COG (chip on glass) structure.

Terukina discloses a liquid crystal display with a chip-on-glass (COG) structure (see Fig. 4) in which the chips for driving the liquid crystal display panel are mounted on a glass substrate (Col. 1, Ln. 14-45). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Hiraki and Mizumaki with the teachings of Terukina in order to implement and fabricate a liquid crystal display panel in which a liquid crystal is sealed between two glass substrates.

21. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiraki et al. (hereinafter "Hiraki" US 6,680,722) in view of Mizumaki (US 6,333,727) and further in view of Montalbo (US 6,356,260).

22. As pertaining to **Claim 11**, Hiraki in view of Mizumaki disclose the liquid crystal display of claim 1. Hiraki teaches that the image data is transmitted to the data driver. However, Hiraki in view of Mizumaki does not teach that the image data is transmitted to the data driver by RSDS (reduced swing differential signaling).

Montalbo discloses a liquid crystal display in which reduced swing differential signaling (RSDS) is utilized to transmit pixel data over a data bus from a timing controller to a display driver or a bank of display drivers in order to reduce power consumption in the display panel (Abstract, Col. 5, Ln. 8-18). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to

combine the teachings of Hiraki and Mizumaki with the teachings of Montalbo in order to reduce power consumption in the liquid crystal display by transmitting the image data to the data driver by RSDS (reduced swing differential signaling).

Response to Arguments

23. Applicant's arguments filed 08 October 2007 have been fully considered but they are not persuasive. **Claims 1-3, 5-7, and 10-15** are pending in the application. Of these, **Claims 1, 3, 11, and 12** have been amended. **Claims 2, 5-7, 10, and 13-15** are original. **Claims 4, 8, and 9** have been canceled. The applicant has argued that the references relied upon in the first office action, namely Hiraki et al. (US 6,680,722) and Mizumaki (US 6,333,727), do not disclose that "the timing controller does not provide the nth image data to the data driver when all bits of the nth image data and the (n-1)th image data are equal and complementary to each other." The examiner agrees. However, this limitation is not enabled in the specification and this limitation requires a condition that is not possible. That is, all bits of the nth image data and the (n-1)th image data cannot be both equal and complementary to each other. The limitation "equal" implies that all bits of the nth image data and the (n-1)th image data are the same, while the limitation "complementary" implies that all bits of the nth image data and the (n-1)th image data are opposite (i.e., all of the "0" bits of the nth image data correspond to "1" bits of the (n-1)th image data, and all of the "1" bits of the nth image

data correspond to "0" bits of the (n-1)th image data). This reasoning can be applied to **Claims 1 and 12** as amended by the applicant. As such, the rejection of **Claims 1-3, 5-7, and 10-15** is maintained.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Mandeville whose telephone number is

571-270-3136. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason Mandeville
Examiner
20 November 2007

JMM

ALEXANDER EISEN
SUPERVISORY PATENT EXAMINER